Cmos Sram Circuit Design And Parametric Test In Nano Scaled Technologies Process Aware Sram Design And Test Frontiers In Electronic Testing

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DALTON JORDAN

Proceedings of ICMEET 2017 Springer Nature
In this book, Complementary Metal Oxide Semiconductor (CMOS) devices are extensively discussed. The topics encompass the technology advancement in the fabrication process of metal oxide semiconductor field effect transistors or MOSFETs (which are the fundamental building blocks of CMOS devices) and the applications of transistors in the present and future eras. The book is intended to provide information on the latest technology development of CMOS to researchers, physicists, as well as engineers working in the field of semiconductor transistor manufacturing and design.
Nanometer Variation-Tolerant SRAM Springer Science & Business Media
CMOS Processors and Memories addresses the-state-of-the-art in integrated circuit design in the context of emerging computing systems. New design opportunities in memories and processor are discussed. Emerging materials that can take system performance beyond standard CMOS, like carbon nanotubes, graphene, ferroelectrics and tunnel junctions are explored. CMOS Processors and Memories is divided into two parts: processors and memories. In the first part we start with high performance, low power processor design, followed by a chapter on multi-core processing. They both represent state-of-the-art concepts in current computing industry. The third chapter deals with asynchronous design that still carries lots of promise for future computing needs. At the end we present a “hardware design space exploration” methodology for implementing and analyzing the hardware for the Bayesian inference framework. This particular methodology involves: analyzing the computational cost and exploring candidate hardware components, proposing various custom architectures using both traditional CMOS and hybrid nanotechnology CMOL. The first part concludes with hybrid CMOS-Nano architectures. The second, memory part covers state-of-the-art SRAM, DRAM, and flash memories as well as emerging device concepts. Semiconductor memory is a good example of the full custom design that applies various analog and logic circuits to utilize the memory cell’s device physics. Critical physical effects that include tunneling, hot electron injection, charge trapping (Flash memory) are discussed in detail. Emerging memories like FRAM, PRAM and ReRAM that depend on magnetization, electron spin alignment, ferroelectric effect, built-in potential well, quantum effects, and thermal melting are also described. CMOS Processors and Memories is a must for anyone serious about circuit design for future computing technologies. The book is written by top notch international experts in industry and academia. It can be used in graduate course curriculum.
Digital CMOS Circuit Design CRC Press
In response to tremendous growth and new technologies in the semiconductor industry, this volume is organized into five, information-rich sections. Digital Design and Fabrication surveys the latest advances in computer architecture and design as well as the technologies used to manufacture and test them. Featuring contributions from leading experts, the book also includes a new section on memory and storage in addition to a new chapter on nonvolatile memory technologies. Developing advanced concepts, this sharply focused book— Describes new technologies that have become driving factors for the electronic industry Includes new information on semiconductor memory circuits, whose development best illustrates the phenomenal progress encountered by the fabrication and technology sector Contains a section dedicated to issues related to system power consumption Describes reliability and testability of computer systems Pinpoints trends and state-of-the-art advances in fabrication and CMOS technologies Describes performance evaluation measures, which are the bottom line from the user’s point of view Discusses design techniques used to create modern computer systems, including high-speed computer arithmetic and high-frequency design, timing and clocking, and PLL and DLL design
SRAM Design for Wireless Sensor Networks Springer
Variability is one of the most challenging obstacles for IC design in the nanometer regime. In nanometer technologies, SRAM show an increased sensitivity to process variations due to low-voltage operation requirements, which are aggravated by the strong demand for lower power consumption and cost, while achieving higher performance and density. With the drastic increase in memory densities, lower supply voltages, and higher variations, statistical simulation methodologies become imperative to estimate memory yield and optimize performance and power. This book is an invaluable reference on robust SRAM circuits and statistical design methodologies for researchers and practicing engineers in the field of memory design. It combines state of the art circuit techniques and statistical methodologies to optimize SRAM performance and yield in nanometer technologies. Provides comprehensive review of state-of-the-art, variation-tolerant SRAM circuit techniques; Discusses Impact of device related process variations and how they affect circuit and system performance, from a design point of view; Helps designers optimize memory yield, with practical statistical design methodologies and yield estimation techniques.
Devices and Modelling Springer Science & Business Media
Embedded SRAM memory is a vital component in modern SoCs. More than 80% of the System-on-Chip (SoC) die area is often occupied by SRAM arrays. As such, system reliability and yield is largely governed by the SRAM's performance and robustness. The aggressive scaling trend in CMOS device minimum feature size, coupled with the growing demand in high-capacity memory integration, has imposed the use of minimal size devices to realize a memory bitcell. The smallest 6T SRAM bitcell to date occupies a 0.1um2 in silicon area. SRAM bitcells continue to benefit from an aggressive scaling trend in CMOS technologies. Unfortunately, other system components, such as interconnects, experience a slower scaling trend. This has resulted in dramatic deterioration in a cell's ability to drive a heavily-loaded interconnects. Moreover, the growing fluctuation in device properties due to Process, Voltage, and Temperature (PVT) variations has added more uncertainty to SRAM operation. Thus ensuring the ability of a miniaturized cell to drive heavily-loaded bitlines and to generate adequate voltage swing is becoming challenging. A large percentage of state-of-the-art SoC system failures are attributed to the inability of SRAM cells to generate the targeted bitline voltage swing within a given access time. The use of read-assist mechanisms and current mode sense amplifiers are the two key strategies used to surmount bitline loading effects. On the other hand, new bitcell topologies and cell supply voltage management are used to overcome fluctuations in device properties. In this research we tackled conventional 6T SRAM bitcell limited drivability by introducing new integrated voltage sensing schemes and current-mode sense amplifiers. The proposed schemes feature a read-assist mechanism. The proposed schemes' functionality and superiority over existing schemes are verified using transient and statistical SPICE simulations. Post-layout extracted views of the devices are used for realistic simulation results. Low-voltage operated SRAM reliability and yield enhancement is investigated and a wordline boost technique is proposed as a means to manage the cell's WL operating voltage. The proposed wordline driver design shows a significant improvement in reliability and yield in a 400-mV 6T SRAM cell. The proposed wordline driver design exploit the cell's Dynamic Noise Margin (DNM), therefore boost peak level and boost decay rate programmability features are added. SPICE transient and statistical simulations are used to verify the proposed design's functionality. Finally, at a bitcell-level, we proposed a new five-transistor (5T) SRAM bitcell which shows competitive performance and reliability figures of merit compared to the conventional 6T bitcell. The functionality of the proposed cell is verified by post-layout SPICE simulations. The proposed bitcell topology is designed, implemented and fabricated in a standard ST CMOS 65nm technology process. A 1.2_ 1.2 mm2 multi-design project test chip consisting of four 32-Kbit (256-row x 128-column) SRAM macros with the required peripheral and timing control units is fabricated. Two of the designed SRAM macros are dedicated for this work, namely, a 32-Kbit 5T macro and a 32-Kbit 6T macro which is used as a comparison reference. Other macros belong to other projects and are not discussed in this document.
Low-power, Low-voltage SRAM Circuits Design for Nanometric CMOS Technologies IET
Low-Power Digital VLSI Design: Circuits and Systems addresses both process technologies and device modeling. Power dissipation in CMOS circuits, several practical circuit examples, and low-power techniques are discussed. Low-voltage issues for digital CMOS and BiCMOS circuits are emphasized. The book also provides an extensive study of advanced CMOS subsystem design. A low-power design methodology is presented with various power minimization techniques at the circuit, logic, architecture and algorithm levels. Features: Low-voltage CMOS device modeling, technology files, design rules Switching activity concept, low-power guidelines to engineering practice Pass-transistor logic families Power dissipation of I/O circuits Multi- and low-VT CMOS logic, static power reduction circuit techniques State of the art design of low-voltage BiCMOS and CMOS circuits Low-power techniques in CMOS SRAMS and DRAMS Low-power on-chip voltage down converter design Numerous advanced CMOS subsystems (e.g. adders, multipliers, data path, memories, regular structures, phase-locked loops) with several design options trading power, delay and area Low-power design methodology, power estimation techniques Power reduction techniques at the logic, architecture and algorithm levels More than 190 circuits explained at the transistor level.
Low Power Design Essentials Springer Nature
FPGA Architecture: Survey and Challenges reviews the historical development of programmable logic devices, the fundamental programming technologies that the programmability is built on, and then describes the basic understandings gleaned from research on architectures. It is an invaluable reference for engineers and computer scientists. It is also an excellent primer for senior or graduate-level students in electrical engineering or computer science.
ICSEC 2020 Springer Science & Business Media
This book contains extended and revised versions of the best papers presented at the 22nd IFIP WG 10.5/IEEE International Conference on Very Large Scale Integration, VLSI-SoC 2014, held in Playa del Carmen, Mexico, in October 2014. The 12 papers included in the book were carefully reviewed and selected from the 33 full papers presented at the conference. The papers cover a wide range of topics in VLSI technology and advanced research. They address the current trend toward increasing chip integration and technology process advancements bringing about stimulating new challenges both at the physical and system-design levels, as well as in the test of these systems.
SOI Circuit Design Concepts Springer Science & Business Media
This book comprises select proceedings of the International Conference on VLSI, Communication and Signal processing (VCAS 2018). It looks at latest research findings in VLSI design and applications. The book covers a wide range of topics in electronics and communication engineering, especially in the area of microelectronics and VLSI design, communication systems and networks, and image and signal processing. The contents of this book will be useful to researchers and professionals alike.
Device Design and Applications Springer Science & Business Media
This book is proceedings of the 7th FTRA International Conference on Future Information Technology (FutureTech 2012). The topics of FutureTech 2012 cover the current hot topics satisfying the world-wide ever-changing needs. The FutureTech 2012 is intended to foster the dissemination of state-of-the-art research in all future IT areas, including their models, services, and novel applications associated with their utilization. The FutureTech 2012 will provide an opportunity for academic and industry professionals to discuss the latest issues and progress in this area. In addition, the conference will publish high quality papers which are closely related to the various theories, modeling, and practical applications in many types of future technology. The main scope of FutureTech 2012 is as follows. Hybrid Information Technology Cloud and Cluster Computing Ubiquitous Networks and Wireless Communications Multimedia Convergence Intelligent and Pervasive Applications Security and Trust Computing IT Management and Service Bioinformatics and Bio-Inspired Computing Database and Data Mining Knowledge System and Intelligent Agent Human-centric Computing and Social Networks The FutureTech is a major forum for scientists, engineers, and practitioners throughout the world to present the latest research, results, ideas, developments and applications in all areas of future technologies.
Proceedings of Second International Conference on Smart Energy and Communication Springer Science & Business Media
Success in the development of recent advanced semiconductor device technologies is due to the success of SRAM memory cells. This book addresses various issues for designing SRAM memory cells for advanced CMOS technology. To study LSI design, SRAM cell design is the best materials subject because issues about variability, leakage and reliability have to be taken into account

for the design.
Circuit Design, Layout, and Simulation CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled TechnologiesProcess-Aware SRAM Design and Test
This book gathers selected papers presented at the 2nd International Conference on Smart Energy and Communication (ICSEC 2020), held at Poornima Institute of Engineering and Technology, Jaipur, India, on March 20–21, 2020. It covers a range of topics in electronics and communication engineering and electrical engineering, including analog circuit design, image processing, wireless and microwave communication, optoelectronics and photonic devices, nano-electronics, renewable energy, smart grid, power systems and industry applications.
From technology to circuit Springer Science & Business Media
Praise for CMOS: Circuit Design, Layout, and SimulationRevised Second Edition from the Technical Reviewers "A refreshing industrial flavor. Design concepts are presented as they are needed for 'just-in-time' learning. Simulating and designing circuits using SPICE is emphasized with literally hundreds of examples. Very few textbooks contain as much detail as this one. Highly recommended!" --Paul M. Furth, New Mexico State University "This book builds a solid knowledge of CMOS circuit design from the ground up. With coverage of process integration, layout, analog and digital models, noise mechanisms, memory circuits, references, amplifiers, PLLs/DLLs, dynamic circuits, and data converters, the text is an excellent reference for both experienced and novice designers alike." --Tyler J. Gomm, Design Engineer, Micron Technology, Inc. "The Second Edition builds upon the success of the first with new chapters that cover additional material such as oversampled converters and non-volatile memories. This is becoming the de facto standard textbook to have on every analog and mixed-signal designer's bookshelf." --Joe Walsh, Design Engineer, AMI Semiconductor CMOS circuits from design to implementation CMOS: Circuit Design, Layout, and Simulation, Revised Second Edition covers the practical design of both analog and digital integrated circuits, offering a vital, contemporary view of a wide range of analog/digital circuit blocks, the BSIM model, data converter architectures, and much more. This edition takes a two-path approach to the topics: design techniques are developed for both long- and short-channel CMOS technologies and then compared. The results are multidimensional explanations that allow readers to gain deep insight into the design process. Features include: Updated materials to reflect CMOS technology's movement into nanometer sizes Discussions on phase- and delay-locked loops, mixed-signal circuits, data converters, and circuit noise More than 1,000 figures, 200 examples, and over 500 end-of-chapter problems In-depth coverage of both analog and digital circuit-level design techniques Real-world process parameters and design rules The book's Web site, CMOSedu.com, provides: solutions to the book's problems; additional homework problems without solutions; SPICE simulation examples using HSPICE, LTspice, and WinSpice; layout tools and examples for actually fabricating a chip; and videos to aid learning
Variation-Aware Advanced CMOS Devices and SRAM CreateSpace
CMOS Memory Circuits is a systematic and comprehensive reference work designed to aid in the understanding of CMOS memory circuits, architectures, and design techniques. CMOS technology is the dominant fabrication method and almost the exclusive choice for semiconductor memory designers. Both the quantity and the variety of complementary-metal-oxide-semiconductor (CMOS) memories are staggering. CMOS memories are traded as mass-products worldwide and are diversified to satisfy nearly all practical requirements in operational speed, power, size, and environmental tolerance. Without the outstanding speed, power, and packing density characteristics of CMOS memories, neither personal computing, nor space exploration, nor superior defense systems, nor many other feats of human ingenuity could be accomplished. Electronic systems need continuous improvements in speed performance, power consumption, packing density, size, weight, and costs. These needs continue to spur the rapid advancement of CMOS memory processing and circuit technologies. CMOS Memory Circuits is essential for those who intend to (1) understand, (2) apply, (3) design and (4) develop CMOS memories.
Low-Power Digital VLSI Design Springer Science & Business Media
Nanotechnology ("nanotech") is the manipulation of matter on an atomic, molecular, and supramolecular scale. The earliest, widespread description of nanotechnology referred to the particular technological goal of precisely manipulating atoms and molecules for fabrication of macroscale products, also now referred to as molecular nanotechnology. A more generalized description of nanotechnology was subsequently established by the National Nanotechnology Initiative, which defines nanotechnology as the manipulation of matter with at least one dimension sized from 1 to 100 nanometers. This definition reflects the fact that quantum mechanical effects are important at this quantum-realm scale, and so the definition shifted from a particular technological goal to a research category inclusive of all types of research and technologies that deal with the special properties of matter that occur below the given size threshold. It is therefore common to see the plural form "nanotechnologies" as well as "nanoscale technologies" to refer to the broad range of research and applications whose common trait is size. Because of the variety of potential applications (including industrial and military), governments have invested billions of dollars in nanotechnology research. Through its National Nanotechnology Initiative, the USA has invested 3.7 billion dollars. The European Union has invested[when?] 1.2 billion and Japan 750 million dollars.
Emerging Trends in Photonics, Signal Processing and Communication Engineering Springer Science & Business Media
The volume contains 94 best selected research papers presented at the Third International Conference on Micro Electronics, Electromagnetics and Telecommunications (ICMEET 2017) The conference was held during 09-10, September, 2017 at Department of Electronics and Communication Engineering, BVRIT Hyderabad College of Engineering for Women, Hyderabad, Telangana, India. The volume includes original and application based research papers on microelectronics, electromagnetics, telecommunications, wireless communications, signal/speech/video processing and embedded systems.
Microelectronics, Circuits and Systems Now Publishers Inc
Variability is one of the most challenging obstacles for IC design in the nanometer regime. In nanometer technologies, SRAM show an increased sensitivity to process variations due to low-voltage operation requirements, which are aggravated by the strong demand for lower power consumption and cost, while achieving higher performance and density. With the drastic increase in memory densities, lower supply voltages, and higher variations, statistical simulation methodologies become imperative to estimate memory yield and optimize performance and power. This book is an invaluable reference on robust SRAM circuits and statistical design methodologies for researchers and practicing engineers in the field of memory design. It combines state of the art circuit techniques and statistical methodologies to optimize SRAM performance and yield in nanometer technologies. Provides comprehensive review of state-of-the-art, variation-tolerant SRAM circuit techniques; Discusses Impact of device related process variations and how they affect circuit and system performance, from a design point of view; Helps designers optimize memory yield, with practical statistical design methodologies and yield estimation techniques.
Robust SRAM Designs and Analysis Springer Science & Business Media
This book provides a comprehensive overview of contemporary issues in complementary metal-oxide semiconductor (CMOS) device design, describing how to overcome process-induced random variations such as line-edge-roughness, random-dopant-fluctuation, and work-function variation, and the applications of novel CMOS devices to cache memory (or Static Random Access Memory, SRAM). The author places emphasis on the physical understanding of process-induced random variation as well as the introduction of novel CMOS device structures and their application to SRAM. The book outlines the technical predicament facing state-of-the-art CMOS technology development, due to the effect of ever-increasing process-induced random/intrinsic variation in transistor performance at the sub-30-nm technology nodes. Therefore, the physical understanding of process-induced random/intrinsic variations and the technical solutions to address these issues plays a key role in new CMOS technology development. This book aims to provide the reader with a deep understanding of the major random variation sources, and the characterization of each random variation source. Furthermore, the book presents various CMOS device designs to surmount the random variation in future CMOS technology, emphasizing the applications to SRAM.
VLSI-SoC: Internet of Things Foundations Springer Science & Business Media
This book features various, ultra low energy, variability resilient SRAM circuit design techniques for wireless sensor network applications. Conventional SRAM design targets area efficiency and high performance at the increased cost of energy consumption, making it unsuitable for computation-intensive sensor node applications. This book, therefore, guides the reader through different techniques at the circuit level for reducing energy consumption and increasing the variability resilience. It includes a detailed review of the most efficient circuit design techniques and trade-offs, introduces new memory architecture techniques, sense amplifier circuits and voltage optimization methods for reducing the impact of variability for the advanced technology nodes.
Timing Performance of Nanometer Digital Circuits Under Process Variations John Wiley & Sons
This is an up-to-date treatment of the analysis and design of CMOS integrated digital logic circuits. The self-contained book covers all of the important digital circuit design styles found in modern CMOS chips, emphasizing solving design problems using the various logic styles available in CMOS.