Synopsys Timing Constraints And Optimization User Guide

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HOOPER DRAKE

Springer Science & Business Media
th Welcome to the proceedings of PATMOS 2007, the 17 in a series of international workshops. PATMOS 2007 was organized by Chalmers University of Technology with IEEE Sweden Chapter of the Solid-State Circuit Society technical - sponsorship and IEEE CEDA sponsorship. Over the years, PATMOS has evolved into an important European event, where - searchers from both industry and academia discuss and investigate the emerging ch- lenges in future and contemporary applications, design methodologies, and tools - quired for the development of the upcoming generations of integrated circuits and systems. The technical program of PATMOS 2007 consisted of state-of-the-art te- nical contributions, three invited talks and an industrial session on design challenges in real-life projects. The technical program focused on timing, performance and power consumption, as well as architectural aspects with particular emphasis on m- eling, design, characterization, analysis and optimization in the nanometer era. The Technical Program Committee, with the assistance of additional expert - viewers, selected the 55 papers presented at PATMOS. The papers were organized into 9 technical sessions and 3 poster sessions. As is always the case with the PATMOS workshops, full papers were required, and several reviews were received per manuscript.

The Art of Timing Closure Springer
The Art of Timing Closure is written using a hands-on approach to describe advanced concepts and techniques using Multi-Mode

Multi-Corner (MMMC) for an advanced ASIC design implementation. It focuses on the physical design, Static Timing Analysis (STA), formal and physical verification. The scripts in this book are based on Cadence® Encounter SystemTM. However, if the reader uses a different EDA tool, that tool's commands are similar to those shown in this book. The topics covered are as follows: Data Structures Multi-Mode Multi-Corner Analysis Design Constraints Floorplan and Timing Placement and Timing Clock Tree Synthesis Final Route and Timing Design Signoff Rather than go into great technical depth, the author emphasizes short, clear descriptions which are implemented by references to authoritative manuscripts. It is the goal of this book to capture the essence of physical design and timing analysis at each stage of the physical design, and to show the reader that physical design and timing analysis engineering should be viewed as a single area of expertise. This book is intended for anyone who is involved in ASIC design implementation -- starting from physical design to final design signoff. Target audiences for this book are practicing ASIC design implementation engineers and students undertaking advanced courses in ASIC design.

19th International Workshop, PATMOS 2009, Delft, The Netherlands, September 9-11, 2009, Revised Selected Papers Springer Science & Business Media

Welcome to the proceedings of PATMOS 2008, the 18th in a series of int- national workshops. PATMOS 2008 was organized by INESC-ID / IST - TU Lisbon, Portugal, with sponsorship by Cadence, IBM, Chipidea, and Tecmic, and technical co-sponsorship by the IEEE. Over the years, PATMOS has evolved into an important European event, where researchers from both industry and academia discuss and investigate the emerging challenges in future and contemporary applications, design meth- ologies, and tools required for the development of the upcoming generations of integrated circuits and systems. The technical program of PATMOS 2008 c- tained state-of-the-art technical contributions, three invited talks, and a special session on recon?gurable architectures. The technical program focused on t- ing, performance and power consumption, as well as architectural aspects with particular emphasis on modeling, design, characterization, analysis and op- mization in the nanometer era. The Technical Program Committee, with the assistance of additional expert reviewers, selected the 41 papers presented at PATMOS. The papers were - ganized into 7 oral sessions (with a total of 31 papers) and 2 poster sessions (with a total of 10 papers). As is customary for the PATMOS workshops, full papers were required for review, and a minimum of three reviews were received per manuscript.

Logic Synthesis and SOC Prototyping Springer Science & Business Media

Achieve enhanced performance with this guide to cutting-edge techniques for digitally-assisted analog and analog-assisted digital integrated circuit design. • Discover how architecture and circuit innovations can deliver improved performance in terms of speed, density, power, and cost • Learn about practical design considerations for high-performance scaled CMOS processes, FinFet devices and architectures, and the implications of FD SOI technology • Get up to speed with established circuit techniques that take advantage of scaled CMOS process technology in analog, digital, RF and SoC designs, including digitally-assisted

techniques for data converters, DSP enabled frequency synthesizers, and digital controllers for switching power converters. With detailed descriptions, explanations, and practical advice from leading industry experts, this is an ideal resource for practicing engineers, researchers, and graduate students working in circuit design.
Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation Springer Science & Business Media
Constraining Designs for Synthesis and Timing AnalysisA Practical Guide to Synopsys Design Constraints (SDC)Springer Science & Business Media
Leakage Power Analysis and Optimization in Deep-Submicron Technologies Under Process Variation Springer Science & Business Media
Logic Synthesis Using Synopsys®, Second Edition is for anyone who hates reading manuals but would still like to learn logic synthesis as practised in the real world. Synopsys Design Compiler, the leading synthesis tool in the EDA marketplace, is the primary focus of the book. The contents of this book are specially organized to assist designers accustomed to schematic capture-based design to develop the required expertise to effectively use the Synopsys Design Compiler. Over 100 `Classic Scenarios' faced by designers when using the Design Compiler have been captured, discussed and solutions provided. These scenarios are based on both personal experiences and actual user queries. A general understanding of the problem-solving techniques provided should help the reader debug similar and more complicated problems. In addition, several examples and dc_shell scripts (Design Compiler scripts) have also been provided. Logic Synthesis Using Synopsys®, Second Edition is an updated and revised version of the very successful first edition. The second edition covers several new and emerging areas, in addition to improvements in the presentation and contents in all chapters from the first edition. With the rapid shrinking of process geometries it is becoming increasingly important that `physical' phenomenon like clusters and wire loads be considered during the synthesis phase. The increasing demand for FPGAs has warranted a greater focus on FPGA synthesis tools and methodology. Finally, behavioral synthesis, the move to designing at a higher level of abstraction than RTL, is fast becoming a reality. These factors have resulted in the inclusion of separate chapters in the second edition to cover Links to Layout, FPGA Synthesis and Behavioral Synthesis, respectively. Logic Synthesis Using Synopsys®, Second Edition has been written with the CAD engineer in mind. A clear understanding of the synthesis tool concepts, its capabilities and the related CAD issues will help the CAD engineer formulate an effective synthesis-based ASIC design methodology. The intent is also to assist design teams to better incorporate and effectively integrate synthesis with their existing in-house design methodology and CAD tools.
Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation Springer
Recent years have seen rapid strides in the level of sophistication of VLSI circuits. On the performance front, there is a vital need for techniques to design fast, low-power chips with minimum area for increasingly complex systems, while on the economic side there

is the vastly increased pressure of time-to-market. These pressures have made the use of CAD tools mandatory in designing complex systems. Timing Analysis and Optimization of Sequential Circuits describes CAD algorithms for analyzing and optimizing the timing behavior of sequential circuits with special reference to performance parameters such as power and area. A unified approach to performance analysis and optimization of sequential circuits is presented. The state of the art in timing analysis and optimization techniques is described for circuits using edge-triggered or level-sensitive memory elements. Specific emphasis is placed on two methods that are true sequential timing optimizations techniques: retiming and clock skew optimization. Timing Analysis and Optimization of Sequential Circuits covers the following topics: Algorithms for sequential timing analysis Fast algorithms for clock skew optimization and their applications Efficient techniques for retiming large sequential circuits Coupling sequential and combinational optimizations. Timing Analysis and Optimization of Sequential Circuits is written for graduate students, researchers and professionals in the area of CAD for VLSI and VLSI circuit design.

Advanced ASIC Chip Synthesis Springer

The second of two volumes in the Electronic Design Automation for Integrated Circuits Handbook, Second Edition, Electronic Design Automation for IC Implementation, Circuit Design, and Process Technology thoroughly examines real-time logic (RTL) to GDSII (a file format used to transfer data of semiconductor physical layout) design flow, analog/mixed signal design, physical verification, and technology computer-aided design (TCAD). Chapters contributed by leading experts authoritatively discuss design for manufacturability (DFM) at the nanoscale, power supply network design and analysis, design modeling, and much more. New to This Edition: Major updates appearing in the initial phases of the design flow, where the level of abstraction keeps rising to support more functionality with lower non-recurring engineering (NRE) costs Significant revisions reflected in the final phases of the design flow, where the complexity due to smaller and smaller geometries is compounded by the slow progress of shorter wavelength lithography New coverage of cutting-edge applications and approaches realized in the decade since publication of the previous edition—these are illustrated by new chapters on 3D circuit integration and clock design Offering improved depth and modernity, Electronic Design Automation for IC Implementation, Circuit Design, and Process Technology provides a valuable, state-of-the-art reference for electronic design automation (EDA) students, researchers, and professionals.

Best Practices for Team-based Design Springer Science & Business Media

The microelectronics market, with special emphasis to the production of complex mixed-signal systems-on-chip (SoC), is driven by three main dynamics, time-- market, productivity and managing complexity. Pushed by the progress in na- meter technology, the design teams are facing a curve of complexity that grows exponentially, thereby slowing down the productivity design rate. Analog design automation tools are not developing at the same pace of technology, once custom design, characterized by decisions taken at each step of the analog

design flow, - lies most of the time on designer knowledge and expertise. Actually, the use of - sign management platforms, like the Cadences Virtuoso platform, with a set of - tegrated CAD tools and database facilities to deal with the design transformations from the system level to the physical implementation, can significantly speed-up the design process and enhance the productivity of analog/mixed-signal integrated circuit (IC) design teams. These design management platforms are a valuable help in analog IC design but they are still far behind the development stage of design automation tools already available for digital design. Therefore, the development of new CAD tools and design methodologies for analog and mixed-signal ICs is ess- tial to increase the designer’s productivity and reduce design productivitygap. The work presented in this book describes a new design automation approach to the problem of sizing analog ICs.

Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation Springer Science & Business Media

This book describes best practices for successful FPGA design. It is the result of the author’s meetings with hundreds of customers on the challenges facing each of their FPGA design teams. By gaining an understanding into their design environments, processes, what works and what does not work, key areas of concern in implementing system designs have been identified and a recommended design methodology to overcome these challenges has been developed. This book’s content has a strong focus on design teams that are spread across sites. The goal being to increase the productivity of FPGA design teams by establishing a common methodology across design teams; enabling the exchange of design blocks across teams. Coverage includes the complete FPGA design flow, from the basics to advanced techniques. This new edition has been enhanced to include new sections on System modeling, embedded design and high level design. The original sections on Design Environment, RTL design and timing closure have all been expanded to include more up to date techniques as well as providing more extensive scripts and RTL code that can be reused by readers. Presents complete, field-tested methodology for FPGA design, focused on reuse across design teams; Offers best practices for FPGA timing closure, in-system debug, and board design; Details techniques to resolve common pitfalls in designing with FPGAs.

Advanced ASIC Chip Synthesis Springer

This book constitutes the refereed proceedings of the 21st International Conference on Integrated Circuit and System Design, PATMOS 2011, held in Madrid, Spain, in September 2011. The 34 revised full papers presented were carefully reviewed and selected from numerous submissions. The paper feature emerging challenges in methodologies and tools for the design of upcoming generations of integrated circuits and systems and focus especially on timing, performance and power consumption as well as architectural aspects with particular emphasis on modeling, design, characterization, analysis and optimization.

15th International Workshop, PATMOS 2005, Leuven, Belgium, September 21-23, 2005, Proceedings Springer Science & Business Media

Adoption and Optimization of Embedded and Real-Time Communication Systems presents innovative research on the integration of embedded systems, real-time systems and the

developments towards multimedia technology. This book is essential for researchers, practitioners, scientists, and IT professionals interested in expanding their knowledge of this interdisciplinary field.

22nd International Workshop, PATMOS 2012, Newcastle upon Tyne, UK, September 4-6, 2012, Revised Selected Papers IGI Global

This book constitutes the thoroughly refereed post-conference proceedings of 19th International Workshop on Power and Timing Modeling, Optimization and Simulation, PATMOS 2009, featuring Integrated Circuit and System Design, held in Delft, The Netherlands during September 9-11, 2009. The 26 revised full papers and 10 revised poster papers presented were carefully reviewed and selected from numerous submissions. The papers are organized in topical sections on variability & statistical timing, circuit level techniques, power management, low power circuits & technology, system level techniques, power & timing optimization techniques, self-timed circuits, low power circuit analysis & optimization, and low power design studies.

Timing Analysis and Optimization of Sequential Circuits Springer

Discover innovative tools that pave the way from circuit and physical design to fabrication processing Nano-CMOS Design for Manufacturability examines the challenges that design engineers face in the nano-scaled era, such as exacerbated effects and the proven design for manufacturability (DFM) methodology in the midst of increasing variability and design process interactions. In addition to discussing the difficulties brought on by the continued dimensional scaling in conformance with Moore's law, the authors also tackle complex issues in the design process to overcome the difficulties, including the use of a functional first silicon to support a predictable product ramp. Moreover, they introduce several emerging concepts, including stress proximity effects, contour-based extraction, and design process interactions. This book is the sequel to Nano-CMOS Circuit and Physical Design, taking design to technology nodes beyond 65nm geometries. It is divided into three parts: Part One, Newly Exacerbated Effects, introduces the newly exacerbated effects that require designers' attention, beginning with a discussion of the lithography aspects of DFM, followed by the impact of layout on transistor performance Part Two, Design Solutions, examines how to mitigate the impact of process effects, discussing the methodology needed to make sub-wavelength patterning technology work in manufacturing, as well as design solutions to deal with signal, power integrity, WELL, stress proximity effects, and process variability Part Three, The Road to DFM, describes new tools needed to support DFM efforts, including an auto-correction tool capable of fixing the layout of cells with multiple optimization goals, followed by a look ahead into the future of DFM Throughout the book, real-world examples simplify complex concepts, helping readers see how they can successfully handle projects on Nano-CMOS nodes. It provides a bridge that allows engineers to go from physical and circuit design to fabrication processing and, in short, make designs that are not only functional, but that also meet power and performance goals within the design schedule.

Logic Synthesis Using Synopsys® CRC Press

This book constitutes the refereed proceedings of the 10th International Workshop on Power and Timing Modeling,

Optimization and Simulation, PATMOS 2000, held in GÃ¶ttingen, Germany in September 2000. The 33 revised full papers presented were carefully reviewed and selected for inclusion in the book. The papers are organized in sections on RTL power modeling, power estimation and optimization, system-level design, transistor level design, asynchronous circuit design, power efficient technologies, design of multimedia processing applications, adiabatic design and arithmetic modules, and analog-digital circuit modeling.

16th International Workshop, PATMOS 2006, Montpellier, France, September 13-15, 2006, Proceedings John Wiley & Sons

Covers the statistical analysis and optimization issues arising due to increased process variations in current technologies. Comprises a valuable reference for statistical analysis and optimization techniques in current and future VLSI design for CAD-Tool developers and for researchers interested in starting work in this very active area of research. Written by author who lead much research in this area who provide novel ideas and approaches to handle the addressed issues

VHDL for Designers Springer

A practical guide to help electronics designers and students make the most of VHDL with the latest, most widely-used design tools available.This book presents both the professional and academic side of designing with VHDL, and shows how to take full advantage of VHDL with today's design tools. It contains many worked examples developed with Synopsys, Mentor Graphics and ViewLook tools. It reviews concurrent, sequential and structural VHDL, RAM and ROM development, state machines, and RTL synthesis. Test methodologies and rapid prototyping are covered, as well as examples of quality design and common errors to avoid. End-of-chapter exercises and laboratories are included throughout.For both engineering professionals and students interested in using VHDL as effectively as possible in their environments.

Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation Springer

This book constitutes the refereed proceedings of the 22nd International Conference on Integrated Circuit and System Design, PATMOS 2012, held in Newcastle, UK Spain, in September 2012. The 25 revised full papers presented were carefully reviewed and selected from numerous submissions. The paper feature emerging challenges in methodologies and tools for the design of upcoming generations of integrated circuits and systems, including reconfigurable hardware such as FPGAs. The technical program focus on timing, performance and power consumption as well as architectural aspects with particular emphasis on modeling, design, characterization, analysis and optimization.

RTL Design using VHDL Springer

This book carefully details design tools and techniques for high-performance ASIC design. Using these techniques, the performance of ASIC designs can be improved by two to three times. Important topics include: Improving performance through microarchitecture; Timing-driven floorplanning; Controlling and exploiting clock skew; High performance latch-based design in an ASIC methodology; Automatically identifying and synthesizing complex logic gates; Automated cell sizing to increase performance and reduce power; Controlling process

variation.These techniques are illustrated by designs running two to three times the speed of typical ASICs in the same process generation.

Tools and Techniques for High-Performance ASIC Design CRC Press

Advanced ASIC Chip Synthesis: Using Synopsys® Design Compiler® and PrimeTime® describes the advanced concepts and techniques used for ASIC chip synthesis, formal verification and static timing analysis, using the Synopsys suite of tools. In addition, the entire ASIC design flow methodology targeted for VDSM (Very-Deep-Sub-Micron) technologies is covered in detail. The emphasis of this book is on real-time application of Synopsys tools used to combat various problems seen at VDSM geometries. Readers will be exposed to an effective design methodology for handling complex, sub-micron ASIC designs. Significance is placed on HDL coding styles, synthesis and optimization, dynamic simulation, formal verification, DFT scan insertion, links to layout, and static timing analysis. At each step, problems related to each phase of the design flow are identified, with solutions and work-arounds described in detail. In addition, crucial issues related to layout, which includes clock tree synthesis and back-end integration (links to layout) are also discussed at length. Furthermore, the book contains in-depth discussions on the basics of Synopsys technology libraries and HDL coding styles, targeted towards optimal synthesis solutions. Advanced ASIC Chip Synthesis: Using Synopsys® Design Compiler® and PrimeTime® is intended for anyone who is involved in the ASIC design methodology, starting from RTL synthesis to final tape-out. Target audiences for this book are practicing ASIC design engineers and graduate students undertaking advanced courses in ASIC chip design and DFT techniques. From the Foreword: `This book, written by Himanshu Bhatnagar, provides a comprehensive overview of the ASIC design flow targeted for VDSM technologies using the Synopsis suite of tools. It emphasizes the practical issues faced by the semiconductor design engineer in terms of synthesis and the integration of front-end and back-end tools. Traditional design methodologies are challenged and unique solutions are offered to help define the next generation of ASIC design flows. The author provides numerous practical examples derived from real-world situations that will prove valuable to practicing ASIC design engineers as well as to students of advanced VLSI courses in ASIC design'. Dr Dwight W. Decker, Chairman and CEO, Conexant Systems, Inc., (Formerly, Rockwell Semiconductor Systems), Newport Beach, CA, USA.